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# APPLICATION FOR LETTERS PATENT

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1 CONDUCTIVE CONNECTION FORMING METHODS,  
2 OXIDATION REDUCING METHODS,  
3 AND INTEGRATED CIRCUITS FORMED THEREBY

4 *Ins 91*  
5 TECHNICAL FIELD

6 This invention relates to methods of forming conductive  
7 connections, methods of reducing oxidation, oxidation protection methods,  
8 methods of forming integrated circuit structures, such as conductive  
9 interconnects and wire bonds, and integrated circuits formed thereby.

10  
11 BACKGROUND OF THE INVENTION

12 Several advantages exist for using copper metalization in integrated  
13 circuits, such as semiconductor devices. However, copper metalization  
14 may be more susceptible to oxidation under certain process conditions as  
15 compared to other metals, such as aluminum. Semiconductor devices  
16 often include at least two primary metal layers with interconnections  
17 between such layers. The first metal layer can be a so-called "metal 1"  
18 layer and the second can be a so-called "metal 2" layer.

19 The first metal layer may be formed on a substrate and covered  
20 by a dielectric material, such as silicon dioxide. An opening for an  
21 interconnect may then be formed through the dielectric material to  
22 expose the first metal layer. The opening may be formed by patterning  
23 a layer of photoresist deposited over the dielectric and etching portions

of the dielectric material exposed through the photoresist. A common process for removing photoresist comprises ashing. Such removal of a photoresist exposes the first metal layer to the ashing conditions, potentially oxidizing the first metal layer. Copper is particularly susceptible to oxidation at high temperature processing, such as processing at 200° C or higher.

One method for reducing oxidation of the first metal layer includes forming a layer of silicon nitride over the first metal layer prior to forming dielectric material over the first metal layer. The dielectric material is then processed as indicated above with formation of a photoresist, patterning of the photoresist, etching, and photoresist removal by ashing. However, after etching an opening for a conductive interconnect, a separate etch of the silicon nitride may be used to expose the first metal layer preparatory to forming a conductive interconnect to such layer. A high level of selectivity may often be provided for etching the silicon nitride compared to etching the dielectric material, such as silicon dioxide. The two-step etch process and highly selective etch of silicon nitride add a level of complexity to such processing that is undesirable.

Accordingly, new methods are desired for forming conductive connections between first and second metal layers in semiconductor devices that reduce oxidation of copper without introducing undue complexity to processing.

1 SUMMARY OF THE INVENTIONS:

2 In one aspect of the invention, a conductive connection forming  
3 method includes forming a first layer comprising a first metal on a  
4 substrate and transforming at least a part of the first layer to a  
5 transformed material comprising the first metal and a second substance  
6 different from the first metal. A conductive connection may be formed  
7 to the first layer by way of the transformed material. The method may  
8 further include forming a second layer comprising a second metal  
9 different from the first metal on the first layer. The transformed  
10 material may be an alloy material comprising the first and second metals.  
11 The alloy material may be less susceptible to formation of metal oxide  
12 compared to the first metal. By way of example, transforming the first  
13 layer may comprise annealing the first and second layer. An exemplary  
14 alloy includes an intermetallic. An exemplary first metal comprises  
15 copper, and an exemplary second metal comprises aluminum, titanium,  
16 palladium, magnesium, or two or more such metals.

17 Further, another aspect of the invention includes a conductive  
18 connection forming method wherein a first layer comprising copper is  
19 formed over a substrate. A second layer of a second metal different  
20 from the copper may be formed over the first layer. At least some of  
21 the second metal may be incorporated into an intermetal layer  
22 comprising the second metal and copper. The method further includes  
23 removing at least a portion of any second metal not incorporated into

1 the intermetal layer and exposing the intermetal layer. A conductive  
2 connection may be formed to the intermetal layer.

3 Such methods may be used as oxidation reducing methods or  
4 methods for protecting metal containing material from oxidation during  
5 semiconductor processing. Such methods are also conducive to use in  
6 methods of forming integrated circuit interconnects or integrated circuit  
7 wire bonds.

8 In another aspect of the invention, an integrated circuit includes  
9 a semiconductive substrate, a layer comprising a first metal over the  
10 substrate, and a layer of alloy material within the first metal comprising  
11 layer. The alloy material layer may comprise the first metal and a  
12 second metal different from the first metal. A conductive connection  
13 may be formed on the alloy layer.

#### 14 15 **BRIEF DESCRIPTION OF THE DRAWINGS**

16 Preferred embodiments of the invention are described below with  
17 reference to the following accompanying drawings.

18 Fig. 1 shows a fragmentary sectional view of a semiconductive  
19 wafer at one step of a method according to one aspect of the invention.

20 Fig. 2 shows the semiconductive wafer fragment of Fig. 1 at a  
21 step subsequent to that shown in Fig. 1.

22 Fig. 3 shows the semiconductive wafer fragment of Fig. 1 at a step  
23 subsequent to that shown in Fig. 2.

1 Fig. 4 shows the semiconductive wafer fragment of Fig. 1 at a step  
2 subsequent to that shown in Fig. 3.

3 Fig. 5 shows the semiconductive wafer fragment of Fig. 1 at an  
4 alternative step subsequent to that shown in Fig. 3.

5 Fig. 6 shows the semiconductive wafer fragment of Fig. 1 at a step  
6 subsequent to that shown in Fig. 4.

7 Fig. 7 shows a fragmentary sectional view of a semiconductive  
8 wafer at one step of a method according to another aspect of the  
9 invention.

10 Figs. 8 - 12 each show the semiconductive wafer fragment of  
11 Fig. 7 at successive steps.

12  
13 **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

14 This disclosure of the invention is submitted in furtherance of the  
15 constitutional purposes of the U.S. Patent Laws "to promote the progress  
16 of science and useful arts" (Article 1, Section 8).

17 In one aspect of the present invention, a conductive connection  
18 forming method includes forming a first layer comprising a first metal  
19 on a substrate. In the context of this document, layers or materials  
20 "comprising metal" or "metal-comprising" layers or materials are defined  
21 to mean any layer or material containing at least one metallic element,  
22 regardless of whether the layer or material exhibits metallic properties.  
23 For example, a metal-comprising layer or material may be a metal oxide,

1 nitride, sulfide, or other substance even though such substance might not  
2 exhibit metallic properties.

3 Turning to Fig. 1, a wafer portion 10 is shown having an  
4 insulation layer 12 and a metal-comprising layer 14 formed on insulation  
5 layer 12. Wafer portion 10 of Fig. 1 is one example of a first layer  
6 comprising a first metal formed on a substrate. Metal-comprising layer  
7 14 may be a variety of structures and compositions having a variety of  
8 functions. Metal-comprising layer 14 can comprise copper, aluminum,  
9 another metal, or two or more such metals. Further, layer 14 may  
10 consist essentially of one or more metallic elements, such as the metals  
11 and metal combinations listed above. In alternative to Fig. 1, insulation  
12 layer 12 may comprise other materials, such as semiconductive or  
13 conductive materials. Further, even though Fig. 1 shows metal-comprising  
14 layer 14 and insulation layer 12 as part of wafer portion 10, the  
15 invention is applicable to a variety of substrates and technology areas.  
16 Wafer portion 10 may comprise part of a semiconductor device, an  
17 integrated circuit device, or other devices and apparatuses.

18 In the context of this document, the term "semiconductor  
19 substrate" or "semiconductive substrate" is defined to mean any  
20 construction comprising semiconductive material, including, but not limited  
21 to, bulk semiconductive materials such as a semiconductive wafer (either  
22 alone or in assemblies comprising other materials thereon), and  
23 semiconductive material layers (either alone or in assemblies comprising

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1 other materials). The term "substrate" refers to any supporting  
2 structure, including, but not limited to, the semiconductive substrates  
3 described above.

4 Accordingly, metal-comprising layer 14 may be formed over a  
5 semiconductive substrate. After formation of metal-comprising layer 14,  
6 a second layer comprising a second metal different from the first metal  
7 in metal-comprising layer 14 may be formed on metal-comprising  
8 layer 14. Fig. 2 shows a metal-comprising layer 16, comprising a second  
9 metal, formed on metal-comprising layer 14. Metal-comprising layer 16  
10 may include, for example, aluminum, titanium, palladium, magnesium,  
11 another metal, or two or more such metals. Further, layer 16 may  
12 consist essentially of one or more metallic elements, such as the metals  
13 and metal combinations listed above. Layers 14 and 16 may comprise,  
14 in addition to metallic elements, non-metallic elements, depending on the  
15 particular application of the present invention and processing conditions.  
16 Metal-comprising layer 16 may have a thickness of about 150 to about  
17 800 Angstroms. Preferably, metal-comprising layer 16 may have a  
18 thickness of about 400 to about 500 Angstroms.

19 The present aspect of the invention further includes transforming  
20 at least a part of the first layer to an alloy material comprising the first  
21 and second metals. Alternatively, the present aspect of the invention  
22 may include incorporating at least some of the second metal into an  
23 alloy layer comprising the second metal and the first metal. The



1 indicated transforming may comprise annealing the first and second layer.  
2 Similarly, the indicated incorporating may also comprise annealing the  
3 first and second layer. Annealing may occur at a temperature of about  
4 400° C to about 500°C. The alloy material may consist essentially of the  
5 first and second metals. Also, the alloy material may comprise an  
6 intermetallic material. In the context of this document, an  
7 "intermetallic" material is a type of metal alloy wherein the constituents  
8 are held together by metallic bonding. Alloys also include other  
9 materials that are not held together by metallic bonding. An  
10 intermetallic material may exhibit properties as described below that are  
11 advantageous in the present invention. However, it is also conceivable  
12 that alloys may exist that exhibit similar properties, but are not  
13 intermetals. Although the aspects of the invention are discussed herein  
14 primarily with reference to intermetals, one of ordinary skill will  
15 appreciate that alloys that are not intermetals may also be suitable.

16 Turning to Fig. 3, an intermetallic material 18 is shown as a result  
17 of transforming part of metal-comprising layer 16 to an intermetallic  
18 material comprising the first and second metals of layers 14 and 16,  
19 respectively. In the present aspect of the invention, about 50 to about  
20 300 Angstroms of metal-comprising layer 14 may be transformed to the  
21 intermetallic material or, preferably, about 150 Angstroms. A variety of  
22 thicknesses for intermetallic material 18 are conceivable and may be  
23 desired, depending on the application of the invention as described

1 herein or otherwise. Fig. 3 shows that intermetallic material 18 exists  
2 beyond the original thickness of first metal layer 14. It is also  
3 conceivable that forming intermetallic material 18 will not add  
4 substantially to the original thickness of first metal layer 14.

5 It is preferred that intermetallic material 18 consist essentially of  
6 the first metal of layer 14 and the second metal of layer 16. It is also  
7 preferred that intermetallic material 18, or another alloy material, exhibit  
8 the property of being less susceptible to the formation of metal oxide  
9 in comparison to the first metal of layer 14. Such a property, as well  
10 as other properties, may allow intermetallic material 18 to reduce  
11 oxidation of metal-comprising layer 14 during subsequent processing.  
12 Oxidation of metal-comprising layer 14 can potentially reduce the  
13 conductivity of conductive connections formed to metal-comprising  
14 layer 14. Accordingly, the present aspect of the invention further  
15 includes forming a conductive connection to the intermetallic material,  
16 or another alloy material. Examples of a conductive connection include  
17 an integrated circuit interconnect, an integrated circuit wire bond, and  
18 other structures.

19 Intermetallic material 18, or another alloy material, may also  
20 advantageously exhibit the property of having approximately the same  
21 resistivity as metal-comprising layer 14. Examples of particularly  
22 advantageous intermetallic materials include intermetals of titanium or  
23 aluminum with copper, specifically,  $\text{TiCu}_3$ . Such intermetals exhibit

approximately the same resistivity as copper. Such intermetals are also much less susceptible to formation of metal oxide compared to copper. Accordingly, providing such intermetals as intermetallic material 18 may reduce the oxidation of copper in processing subsequent to formation of such intermetal.

Depending on the particular application of the invention, it may be desirable to remove some portion of metal-comprising layer 16, intermetallic material 18, and/or metal-comprising layer 14. A variety of processing scenarios are conceivable. For example, substantially all of metal-comprising layer 16 not comprised by intermetallic material 18 may be removed. Figs. 4 and 5 both present examples of such removal. In Fig. 4, the portion of intermetallic material 18 beyond the original thickness of metal-comprising layer 14 is shown removed along with substantially all of metal-comprising layer 16. Such a removal leaves behind only the portion of intermetallic material 18 formed within metal-comprising layer 14. Such removal may be accomplished by a variety of processes.

A non-selective etch or chemical mechanical polishing are two examples of potential processes. As shown in Fig. 4, such processes, as well as other processes, may be used to also remove any portion of metal-comprising layer 16 not comprised by the intermetallic material. Removing "substantially" all of a material may allow insignificant portions of such material to remain provided that the central objective of the

1 removal is accomplished. One possible objective for removing metal-  
2 comprising layer 16 is to prevent electrical shorts between other  
3 conductive structures, such as the two portions of metal-comprising layer  
4 14 shown in Figs. 1 - 6.

5 In alternative to the above-described methods, the objective of  
6 avoiding electrical shorts, as well as other objectives, may be met by  
7 instead removing at least some of metal-comprising layer 16 not  
8 comprised by intermetallic material 18. A sufficient thickness of  
9 intermetallic material 18 may be left behind to reduce oxidation of  
10 metal-comprising layer 14. The potential additional objective of exposing  
11 intermetallic material 18 may be met by such an alternative process as  
12 well as by the other previously mentioned processes for removing metal-  
13 comprising layer 16.

14 Turning to Fig. 5, an alternative structure is shown that may result  
15 from the latter-mentioned processes for removing metal-comprising layer  
16 16. In Fig. 5, substantially all of metal-comprising layer 16 is removed  
17 without removing a substantial portion of intermetallic material 18. Not  
18 removing a "substantial" portion at a material means that if any removal  
19 occurs, such removal is not sufficient to prevent the central objective of  
20 providing such material. Such a removal process may be accomplished  
21 by a selective etch of metal-comprising layer 16 in preference to  
22 intermetallic material 18. The selectivity ratio of layer 16 removal to  
23 material 18 removal may greater than 5 to 1, for example, approximately

10 or more to 1. One potential selective etch includes exposure of metal-comprising layer 16 to a halogenated acid, such as HF or HCl, or other acids, such as H<sub>2</sub>SO<sub>4</sub> and HNO<sub>3</sub>, or combinations thereof. Such exposure may be effective to remove either titanium or aluminum metal substantially selectively to copper intermetals with titanium or aluminum. A conductive connection may then be formed to the exposed intermetal material 18 as described above. It is also conceivable within the present aspect of the invention that some portion of metal-comprising layer 16 will remain, rather than removing substantially all of such material. For example, only a portion of metal-comprising layer 16 sufficient to expose intermetallic material 18 may be removed, still allowing formation of a conductive connection.

Another aspect of the invention includes an oxidation reducing method wherein a layer comprising a first metal may be contacted with a second metal different from the first metal while treating the layer in contact with the second metal. The method includes forming an intermetallic material at least partially within the layer, the intermetallic material comprising the first and second metals. Further, substantially all of any residual second metal not comprised by the intermetallic material may be removed from over the intermetallic material. A conductive connection to the intermetallic material may be formed without forming a substantial amount of metal oxide on the first metal. Treating the layer in contact with the second metal may comprise

annealing the layer. From the text associated with Figs. 1-5 above, it can be seen that such figures provide one example of an oxidation reducing method.

In an oxidation protection method, also exemplified by Figs. 1-5, metal-containing material may be protected during semiconductor processing. A first metal-containing material may be formed over a substrate followed by a second metal-containing material over the first metal-containing material. Annealing the first and second metal-containing materials may form an intermetal material from some of the first material and some of the second material. After annealing, the intermetal material may be exposed to conditions effective to oxidize the first metal-containing material, but the intermetal material may protect at least some of the first metal-containing material from oxidation during the exposing.

Turning to Fig. 6, a structure 60 formed by an integrated circuit interconnect forming method is exemplified, illustrating yet another aspect of the invention. In Fig. 6, metal-comprising layer 64 comprises a first level of integrated circuit wiring formed over an insulation layer 62 over a semiconductive substrate (not shown). Intermetallic material 68, or another alloy material, is formed at least partially within such first wiring level and intermetallic material 68 comprises a first metal from metal-comprising layer 64 and a second metal different from the first metal. A conductive interconnect 65 is shown formed through an insulation layer

63 in electrical contact with intermetallic material 68. Conductive interconnect 65 may be formed on intermetallic material 68.

In the present aspect of the invention, forming intermetallic material 68 may comprise forming a layer comprising the second metal on the first wiring level. One example is shown in Fig. 2 wherein metal-comprising layer 16 is formed on metal-comprising layer 14. Forming the intermetallic material may further include annealing the layer and first wiring level and removing at least some of any second metal not comprised by the intermetallic material. A sufficient thickness of intermetallic material may be left behind to reduce oxidation of the first wiring level where conductive interconnect 65 connects to the first wiring level.

Fig. 6 shows conductive interconnect 65 formed from the same material as a second level 66 of integrated circuit wiring. Such a structure may be produced by forming second wiring level 66 over first wiring level 64 during formation of conductive interconnect 65. A dual damascene process or similar process known to those skilled in the art may accomplish formation of such a structure.

Another aspect of the present invention includes an integrated circuit wire bond forming method. Such method involves forming integrated circuit wiring and defining a bond pad in the wiring comprising a first metal. An intermetallic material may be formed at least partially within the bond pad, the intermetallic material comprising

1 the first metal and a second metal different from the first metal. A  
2 wire bond may be formed in electrical contact with the intermetallic  
3 material.

4 Turning to Figs. 7-12, one example of the integrated circuit wire  
5 bond forming method is illustrated. Fig. 7 shows a wafer portion 70  
6 including an insulation layer 72 and integrated circuit wiring 78 formed  
7 in insulation layer 72. Opening 74 formed in insulation layer 72 exposes  
8 a portion of integrated circuit wiring to allow formation of additional  
9 wiring within opening 74. Opening 76 is formed in insulation layer 72,  
10 exposing integrated circuit wiring 78 to allow formation of a bond pad.  
11 In Fig. 8, bond pad opening 76 is extended further into insulation  
12 layer 72 forming extended bond pad opening 80. In Fig. 9, a layer of  
13 conductive material 82 comprising a first metal is formed over wafer  
14 portion 70 to provide conductive material for additional wiring in wiring  
15 opening 74 and a bond pad in extended bond pad opening 80.

16 As shown in Fig. 10, a layer 84 comprising a second metal may  
17 be formed over conductive layer 82. Formation of second-metal-  
18 comprising layer 84 allows formation of an intermetallic material at least  
19 partially within the portion of conductive layer 82 within extended bond  
20 pad opening 80. Formation of an intermetallic material may be  
21 accomplished within extended bond pad opening 80 using processes as  
22 described herein. In one such process, layer 84 and conductive layer 82  
23 within bond pad opening 80 are annealed. Such annealing produces



1 wafer portion 70 shown in Fig. 11 having intermetallic material 86, or  
2 another alloy material, at least partially within conductive layer 82 within  
3 bond pad opening 80. At least some of any second metal not comprised  
4 by the intermetallic material may be removed, leaving a sufficient  
5 thickness of intermetallic material to reduce oxidation of a bond pad  
6 where a wire bond contacts such bond pad.

7 In Fig. 11, substantially all of second-metal-comprising layer 84 is  
8 comprised by intermetallic material 86. Such a feature may be practiced  
9 with any of the aspects of the invention disclosed herein. That is,  
10 substantially all of a thickness of a layer comprising a second metal that  
11 exists over a layer comprising a first metal may be transformed to an  
12 intermetallic material. In this manner, only intermetallic material, rather  
13 than excess second metal from the second-metal-comprising layer will  
14 exist over a first-metal-comprising layer.

15 Turning to Fig. 12, excess portions of intermetallic material 86 and  
16 conductive layer 82 are shown removed from wafer portion 70. Such  
17 removal forms additional integrated circuit wiring 88 from conductive  
18 layer 82 within wiring opening 74. Such removal also forms bond  
19 pad 90 from intermetallic material 86 and conductive layer 82 within  
20 bond pad opening 80. At least one of the effects of extending bond  
21 pad opening 76 into insulation layer 72 is formation of bond pad 90  
22 having an outer surface that is topographically below immediately  
23 surrounding structures. By extending bond pad opening 76 less deep

1 into insulation layer 72, the outer surface of bond pad 90 may be made  
2 level with immediately surrounding structures but still comprise  
3 intermetallic material 86. Defining a bond pad as described may provide  
4 easy removal of intermetallic material 86 by planarization methods, for  
5 example chemical mechanical polishing, from all areas except over  
6 conductive layer 82 within bond pad opening 80.

7 As also seen in Figs. 9-12, such processing also provides  
8 intermetallic material 86 at least partially within bond pad 90. As  
9 discussed above regarding other aspects of the invention, intermetallic  
10 material may exhibit a property of resistance to oxidation during  
11 semiconductor processing. Accordingly, formation of conductivity limiting  
12 metal oxide may be reduced when forming a wire bond 92 to bond  
13 pad 90. Such is even true when bond pad 90 and wire bond 92  
14 comprise copper.

15 In the aspects of the invention described above, a transformed  
16 material, such as an alloy material or another material, may be formed  
17 by still other methods. A conductive connection forming method can  
18 include transforming at least a part of metal-comprising layer 14 to a  
19 transformed material by ion implanting. Implanting a second substance  
20 different from the metal in metal-comprising layer 14 may impart a  
21 decreased susceptibility in the transformed material to oxidation compared  
22 to the metal. For example, nitrogen or another substance may be  
23 implanted into metal-comprising layer 14 to an extent sufficient to

1 decrease oxidation. The nitrogen implant may be sufficiently limited in  
2 amount and depth such that a conductive connection may still be formed  
3 to the metal-comprising layer 14 by way of the transformed material.  
4 Limiting the implant energy may produce a shallow implant of metal-  
5 comprising layer 14, thus also limiting any impact on conductivity of  
6 metal-comprising layer 14.

7 In compliance with the statute, the invention has been described  
8 in language more or less specific as to structural and methodical  
9 features. It is to be understood, however, that the invention is not  
10 limited to the specific features shown and described, since the means  
11 herein disclosed comprise preferred forms of putting the invention into  
12 effect. The invention is, therefore, claimed in any of its forms or  
13 modifications within the proper scope of the appended claims  
14 appropriately interpreted in accordance with the doctrine of equivalents.  
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